

## Tuesday, Aug. 21, 2018 - Agenda Schedule

08:00		<b>Continental Breakfast</b>	
08:25	<b>S-3</b>	Presentation Introductions	Jim Devereaux, Xilinx FAE
		<b>Keynote Address</b>	
08:30	<b>S-4</b>	Insights into Three(-plus) Decades of FPGAs	Steve Trimberger, self (Xilinx retired)
		<b>Session F: Infrastructure: Software, IP, &amp; Methodology</b>	
09:20	<b>F3</b>	GUIs: FuncMon, ConfigMon, & FaultMon	Gary Swift, Swift ERS
09:40	<b>F4</b>	TURTLE Fault Injection Infrastructure & Results	Prof. Mike Wirthlin, BYU
10:00	<b>F5</b>	Using Python for XRTC Data Analysis	Gary Swift, Swift ERS
10:20		<b>BREAK</b>	
		<b>Session T: Topics of Interest</b>	
10:30	<b>T4</b>	Test H/W sans RTL: Pynq Board Overview	Patrick Lysaght, Xilinx
		<b>Session A: Test Results</b>	
11:00	<b>A5</b>	V7 : BRAMs & BRAM-ECC	Bill Rowe, Raytheon
11:20	<b>A6</b>	V7 : BRAMs & Config Multi Cell Upsets	Prof. Mike Wirthlin, BYU
11:40	<b>A7</b>	US+ : Config, BRAM, & Flip-Flops	David Lee, Sandia
		<b>Session B: Projects and Missions</b>	
12:00	<b>B3</b>	Framework for On-orbit Reconfiguration	Christopher Stender, Fraunhofer IIS
12:30		<b>LUNCH</b>	
13:10	<b>T5</b>	Concurrent Tracks: Vivado Tutorial & Demo – Main Room	Jim Devereaux, Xilinx FAE
13:10	<b>NDA</b>	Concurrent Tracks: KU060 TID (NDA only) – Side Room	Pierre Maillard, Xilinx Technology Development
		<b>Session E: Ecosystem</b>	
13:50	<b>E4</b>	KU060 & V5 Adjunct Space Parts/Solutions	Javier Valle, TI
14:10	<b>E5</b>	Memory Infrastructure for Space FPGAs	Helmut Puchner, Cypress
		<b>Session B: Projects and Missions</b>	
14:30	<b>B4</b>	tba	
		<b>Session C: Infrastructure: Hardware and Boards</b>	
14:50	<b>C5</b>	Details: BrainBox Operation	Gary Swift, Swift ERS
15:10		<b>BREAK</b>	
15:30	<b>C6</b>	Details: SMAP JCM Capabilities & Tools	Prof. Mike Wirthlin, BYU
16:00	<b>C7</b>	Looking Ahead: Gen4 Improvements	Gary Swift, Swift ERS
16:10	<b>C8</b>	Status: FMC-based, Motherboard-less Concept	David Lee, Sandia
		<b>Session T: Topics of Interest</b>	
16:30	<b>T6</b>	Fitting Thinned Die via Kriging *	Sebastian Garcia, S-Labs
		<b>Session D: Test Planning</b>	
16:50	<b>D3</b>	Misc'l: V7 Primitives, Processors, Mitigation	Gary Swift, Swift ERS
17:05	<b>D4</b>	Flight Designs : In-Beam Test Capability	Gary Swift, Swift ERS
17:20		<b>--- END of Day 2 ---</b>	